Minimum thickness control at various levels for topology optimization using the wavelet method

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Abstract

Especially in microsystem design, maintaining the minimum thickness of each structural member at a certain scale is often as important as achieving the maximum system performance. Several successful methods to suppress one-point hinges or checkerboards in topology optimization have been developed, but an efficient method to control the minimum thickness at a desire scale remains to be developed. The objective of this investigation is to develop a wavelet-based minimum thickness controlling method applicable to topology optimization and to show the effectiveness of the proposed method in MEMS design. The idea behind the thickness controlling method is to extend the wavelet shrinkage method developed for one-point hinge control to any scale-level minimum thickness control. The major difficulties in implementing this idea are the development of an efficient algorithm to detect all undesirable patterns of different scales and the hierarchical application of the wavelet shrinkage method over multiple scales. Some techniques to overcome these difficulties are developed and applied to some MEMS design problems.
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Keywords: Topology optimization; Minimum thickness; Wavelet method; MEMS design

1. Introduction

In most engineering design, not only system performance but also manufacturing cost is important. Based on an observation that the minimum member-thickness issue is a primary factor affecting

manufacturing cost, we investigate the minimum thickness controlling scheme for topology optimization. The specific application in consideration is MEMS design.

1.1. Thickness-related issue in MEMS design

Especially in MEMS design, some processing techniques cannot handle structures whose aspect ratios are higher than certain values or structures whose member sizes are smaller than certain scales (see Jonsmann, 1999; Bertz et al., 2002; Ayazi and Najafi, 2002; Elwenspoek and Wiegerink, 2001).

To address the thickness issue in MEMS design, we actually manufactured an electro-thermal-compliant actuator in Fig. 1(a) that was optimized by topology optimization. For the design in Fig. 1, no minimum member size control was considered. During actuation tests, only a few percentages of the manufactured actuators survived. A typical failure is illustrated in Fig. 1(d) and it is found that the failure occurred where the member was very thin. This observation has called for the consideration of not only system performance but also minimum member control during the topology optimization of the actuator.

1.2. Scale and minimum thickness in topology optimization

Let us now consider how the minimum thickness issue or the scale issue has been addressed in topology optimization. To address this issue, three patterns of structural connectivity shown in Fig. 2 are considered. Fig. 2(a) shows a well-known one-point hinge connection. If the one-point hinge connections are repeated, the resulting pattern becomes a so-called checkerboard pattern. For subsequent discussion, the one-point hinge connection will be referred to as the connection of thickness 0 (CT0). When CT0 appears as the result of optimization, one may have to replace CT0 as the connections having thickness of 1 (CT1) or 2 (CT2) to avoid failures such as the one shown in Fig. 1(d). Connection CT1 and CT2 are illustrated in Fig. 2(b) and (c). In our discussion, the symbol CTn (n: positive integer) is used to denote a connection of thickness n where the finite element used for analysis is assumed to be square.

When systems to be optimized are in microscales, CTn may need to be replaced by CT$(n+1)$ or CT$(n+2)$. Quite often, this replacement deteriorates the systems performance substantially (see e.g., Jonsmann, 1999). To avoid the excessive system performance drop due to the postprocessed thickening, the
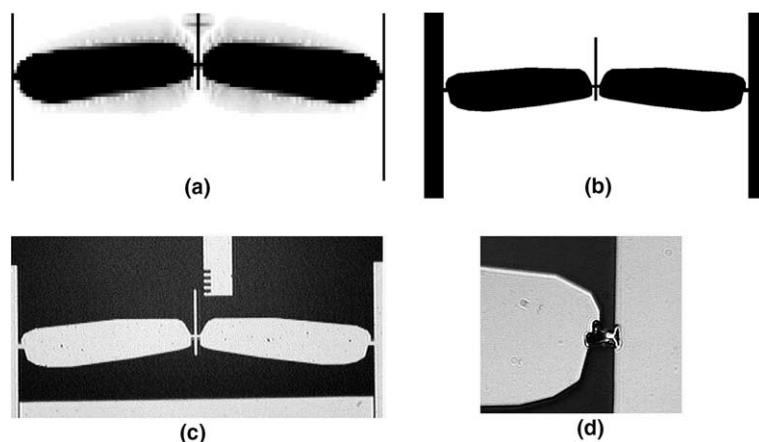

Fig. 1. Optimization and fabrication of an electro-thermal-compliant actuator. (a) A direct numerical result by the topology optimization without any control on the minimum member size, (b) postprocessed result of (a), (c) a successfully fabricated actuator by the MEMS technology, (d) a failed actuator during the fabrication.
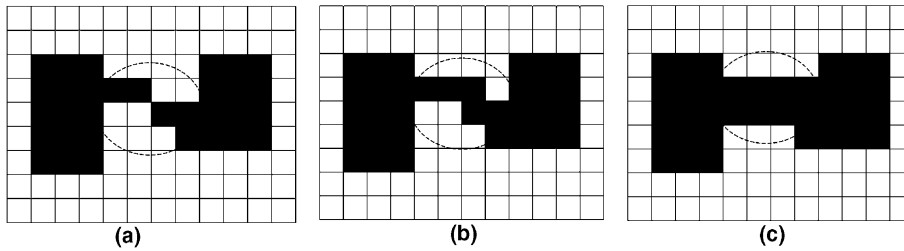
Fig. 2. Various element connections. (a) CT0 (connection of thickness 0), (b) CT1 (connection of thickness 1), (c) CT2 (connection of thickness 2).

minimum size of the structural connection should be taken into account in the topology optimization process.

The interest in the size issue in topology optimization goes back to Harber et al. (1996) who developed the perimeter controlling method. A method to constrain slopes-constrained optimization was also developed by Petersson and Sigmund (1998). The minimum length-scale imposing scheme was developed by Zhou et al. (2001) and the length control over a few scale levels was proposed by Poulsen (2003). However, he treated the minimum thickness as the constraint equation.

The objective of this investigation is twofold: to develop an efficient wavelet-based method to impose the minimum connection thickness at various scale levels and to apply the method to the design of MEMS, such as microelectro-thermal-compliant actuators, where the minimum thickness control is one of critical issues. The optimization formulations for the design problems considered in this work were given by Sigmund (2001) and Ananthasuresh et al. (1994), but the minimum thickness control was not considered in their investigations.

The wavelet-based method developed in this work restricts the design space by the hierarchical application of non-redundant translation-invariant wavelet shrinkage operations. Unlike Poulsen's method (2003), the wavelet-based method does not treat the minimum thickness control as extra constraint equations. Furthermore, the patterns to be controlled can be defined more easily in the wavelet space than in the direct density space. This design space restriction method by the wavelet shrinkage was developed earlier by Yoon et al. (2004) in which only CT0's, that is, only the one-point hinge connection and checkerboard patterns were controlled.

Since the objective of the present investigation is to eliminate all patterns from CT0 to CTn ($n = 1, 2, \ldots$), wavelet shrinkage operations must be applied hierarchically over several scales. The key step in the development of the hierarchical wavelet shrinkage is to establish the correct condition to suppress CTn over multiple scales. To this end, the patches representing the patterns to be deleted should be declared and a robust hierarchical pattern detection algorithm must be developed. Typical pattern detection algorithms usually employ the logical statements such as "IF," "OR," and "NOT," but they should be made differentiable if one wishes to use them within efficient gradient-based optimizers. Thus, a method to replace all the logical operations by approximate differentiable logical operations is developed by extending the idea suggested in Yoon et al. (2004). A hierarchical wavelet shrinkage method is then developed by applying the differentiable operators over multiple scales.

As application problems, two MEMS design problems were considered: the design of thermal actuators and the design of electro-thermal-compliant actuators. These problems were studied earlier, but perhaps the present investigation is the first effort to apply the minimum thickness controlling scheme to these problems. We also addressed how optimized design configurations as well as the system performance are affected by the minimum thickness control. We confirmed the effectiveness of the minimum thickness controlling method in the design of an electro-thermal-compliant actuator where some candidate designs were actually fabricated by the MEMS processing technology.

2. Wavelet-based topology optimization method

2.1. Topology optimization

In case of structure-involving topology optimization problems, one can set up the following minimization problem:

$$\text{minimize} \quad \Phi = \Phi(\mathbf{U}, \boldsymbol{\rho})$$

$$\text{subject to} \quad H(\boldsymbol{\rho}) = \sum_{e=1}^{NE} \rho_e v_e - M_0 \leqslant 0 \quad (M_0: \text{Mass limit}) \tag{1}$$

$$\mathbf{KU} = \mathbf{F} \quad (\text{Equilibrium equation})$$

$$\varepsilon \leqslant \boldsymbol{\rho} \leqslant 1 \quad (\varepsilon: \text{small number})$$

where $\mathbf{U}$ is the displacement and $\boldsymbol{\rho}$ are the density design variables defined on finite elements. The number of elements and the element volume are denoted by NE and v_e, respectively. The symbols $\mathbf{K}$ and $\mathbf{F}$ are the stiffness matrix and the load vector, respectively. In the SIMP (Solid Isotropic Material with Penalization) method, the material properties are interpolated as some functions of the density variables. The problem in Eq. (1) is usually solved by mathematical programming. The objective function Φ can be defined for a given design problem (see Bendsøe and Kikuchi, 1988; Bendsøe and Sigmund, 2003).

2.2. Topology optimization in the wavelet design space

In the conventional topology optimization method explained above, a design variable represents the relative density value of a single finite element. However, it would be possible to define a set of design variables that are defined over a different number of finite elements. Namely, the design variables can be expressed in multiple scales. This idea has been used in Kim and Yoon (2000), Poulsen (2002), Yoon et al. (2004), Seo and Kim (2005) and Yoon and Kim (2005). The wavelet method has been called the wavelet-based multiscale topology optimization because wavelets are used for the multiscale transformation.

To compare the single-scale and multiscale representations, consider Fig. 3 showing a design domain discretized by 8×8 mesh. In the usual single-scale setting, 64 single-scaled functions are used to represent the design variables assigned to 64 finite elements, as illustrated in Fig. 3(a). On the other hand, the 64 design variables can also be represented by another set of 64 functions having different support scales as shown in Fig. 3(b). The functions shown in Fig. 3(b) may be referred to as the so-called non-standard two-dimensional Haar wavelets (see Stollnitz et al., 1996).

To avoid the complexity in the multiscale design space resulting from the side constraint imposed on the original density variables, the density design variables $\boldsymbol{\rho}$ are transformed to auxiliary variables $\boldsymbol{\xi}$ which are then transformed to the wavelet variables $\mathbf{W}$ by the non-standard Haar wavelet transform $\boldsymbol{T}$ (see Mallat, 1998). These transformations may be written symbolically as

$$\rho = \frac{1}{1 + e^{\sigma\xi}}, \quad -\infty \leqslant \xi \leqslant \infty \quad (\text{say}, \ \sigma = -0.3) \tag{2}$$

$$\mathbf{W} = \boldsymbol{T}\boldsymbol{\xi} \tag{3}$$

where the symbol $\mathbf{W}$ and $\boldsymbol{\xi}$ stand for the vectors consisting of the wavelet variables and the auxiliary variables respectively. See Seo and Kim (2005) for the matrix description of the wavelet transformation $\boldsymbol{T}$. (Note that the upper-case symbol $\mathbf{W}$ is used to represent the one-dimensional array $\mathbf{W}$ in Seo and Kim (2005).) Fig. 4 schematically describes the mapping procedure from the density variables to the wavelet variables for a density region or a patch consisting of 2×2 finite elements.
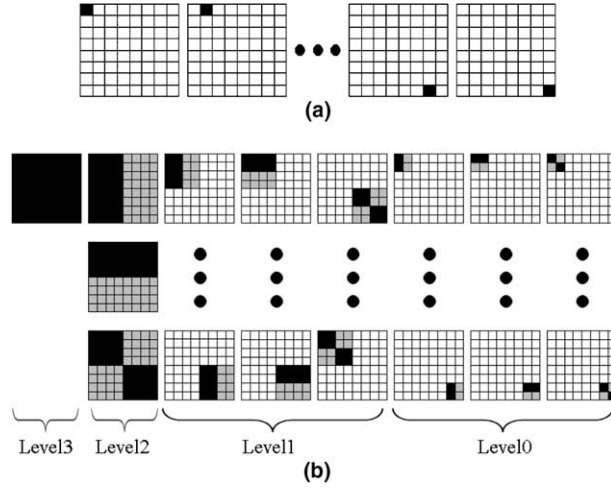
Fig. 3. (a) Single-scale representation, (b) multiscale representation by the non-standard Haar wavelets (Black: Positive; Gray: Negative; White: 0).

For the case described in Fig. 4, the relation between ξ_i and w_i can be written as

$$\begin{Bmatrix} w_1 \\ w_2 \\ w_3 \\ w_4 \end{Bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 & 1 & 1 \\ -1 & 1 & -1 & 1 \\ -1 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \begin{Bmatrix} \xi_1 \\ \xi_2 \\ \xi_3 \\ \xi_4 \end{Bmatrix} \tag{4}$$

After this transformation, the topology optimization of Eq. (1) in the wavelet space is redefined as:

$$\text{minimize} \quad \Phi = \Phi(\mathbf{U}, \mathbf{W})$$

$$\text{subject to} \quad H(\mathbf{W}) = \sum_{e=1}^{NE} \rho_e v_e - M_0 \leqslant 0 \quad (M_0 \text{: Mass limit}) \tag{5}$$

Then the sensitivities of Φ and H with respect to $\mathbf{W}$ becomes (see also Seo and Kim, 2005)

$$\frac{\mathrm{d}\Phi}{\mathrm{d}\mathbf{W}} = \frac{\mathrm{d}\xi}{\mathrm{d}\mathbf{W}} \cdot \frac{\mathrm{d}\boldsymbol{\rho}}{\mathrm{d}\xi} \cdot \frac{\mathrm{d}\Phi}{\mathrm{d}\boldsymbol{\rho}} = \boldsymbol{T} \cdot \frac{\mathrm{d}\boldsymbol{\rho}}{\mathrm{d}\xi} \cdot \frac{\mathrm{d}\Phi}{\mathrm{d}\boldsymbol{\rho}} \tag{6}$$
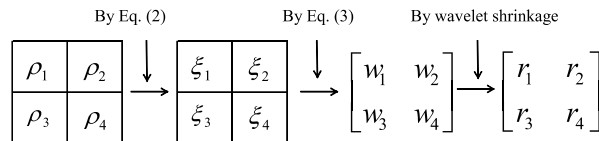

Fig. 4. The schematic procedure for the wavelet shrinkage applied to the wavelet variables $\mathbf{W}$ that are mapped from the density variables $\boldsymbol{\rho}$.

$$\frac{\mathrm{d}H}{\mathrm{d}\mathbf{W}} = \frac{\mathrm{d}\boldsymbol{\xi}}{\mathrm{d}\mathbf{W}} \cdot \frac{\mathrm{d}\boldsymbol{\rho}}{\mathrm{d}\boldsymbol{\xi}} \cdot \frac{\mathrm{d}H}{\mathrm{d}\boldsymbol{\rho}} = \boldsymbol{T} \cdot \frac{\mathrm{d}\boldsymbol{\rho}}{\mathrm{d}\boldsymbol{\xi}} \cdot \frac{\mathrm{d}H}{\mathrm{d}\boldsymbol{\rho}} \tag{7}$$

where

$$\frac{\mathrm{d}\boldsymbol{\rho}}{\mathrm{d}\boldsymbol{\xi}} = -\frac{\sigma \mathrm{e}^{\sigma\xi}}{(1 + \mathrm{e}^{\sigma\xi})^2} \tag{8}$$

2.3. Hinge-free design optimization using the multiscale topology optimization

Now, a wavelet-shrinkage method developed for one-point hinge control (Yoon et al., 2004) will be explained as this method is used as a building block for minimum member thickness control.

2.3.1. Wavelet shrinkage to eliminate CT0 from the $\mathbf{W}$ space

If a 2×2 patch in Fig. 4 is detected as a hinge pattern (CT0), the wavelet variables $\mathbf{W}$ are shrunk or modified to eliminate CT0's. The operating shrinking $\mathbf{W}$ to CT0-free variables, $\mathbf{R}$ in Fig. 4 may be described by an operation sh:

$$
\begin{aligned}
r_1 &= w_1 \quad \text{(no shrinkage)} \\
r_2 &= \mathrm{sh}(w_2, w_3, w_4)w_2 \\
r_3 &= \mathrm{sh}(w_2, w_3, w_4)w_3 \\
r_4 &= \mathrm{sh}(w_2, w_3, w_4)w_4
\end{aligned}
\tag{9}
$$

where

$$\mathrm{sh}(w_2, w_3, w_4) = \begin{cases} 0 & \text{if the patch is a hinge} \\ 1 & \text{else} \end{cases} \tag{10}$$

Since the detailed explanation on the shrinkage operation sh has been given in Yoon et al. (2004), it will not be repeated. However, it is emphasized that the shrinkage operation to suppress CT0 patterns is represented easily with the wavelet variables w_i.

2.3.2. Non-redundant translation-invariant shrinkage

The wavelet transform at the shortest-scale level applies to patches consisting of 2×2 elements, which are translations of each other by two elements in the horizontal, vertical and diagonal directions. For instance, the two-dimensional Haar wavelets representing the diagonal differences may be illustrated as those shown in Fig. 5.

If the wavelets shown in Fig. 5 are used for hinge detection, the patterns shown in Fig. 6 and their translations by even numbers of elements in the horizontal, vertical, or diagonal directions may not be captured by the shrinkage algorithm described earlier. Therefore, the non-redundant translation-invariant wavelet shrinkage algorithm has been developed in order to search all possible hinge patterns.

Fig. 7 schematically compares the standard single-scale approach and the wavelet approaches. In Fig. 7(c), the symbol $\overline{\mathbf{S}}_{\mathrm{D}}^{0}$ denotes the non-redundant translation-invariant operation, the wavelet shrinkage operation developed for the control of CT0 patterns. The meaning of several notations in $\overline{\mathbf{S}}_{\mathrm{D}}^{0}$: such as the superscript 0 will be explained in the next section where more general shrinkage operation $\mathbf{S}$ are developed.
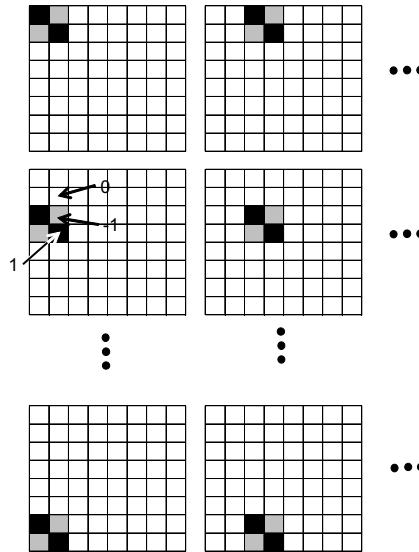
Fig. 5. The illustration of the two-dimensional Haar wavelets representing the shortest-scale diagonal differences.
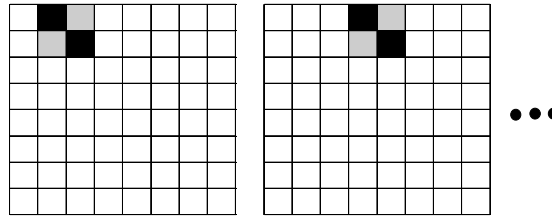

Fig. 6. Translations of the patches in Fig. 5.

3. The development of the hierarchical wavelet shrinkage method for various minimum thickness controls

In this section, a wavelet shrinkage method by Yoon et al. (2004) will be generalized for CT0 control for the control of CTn patterns with $n \geqslant 1$. The proposed CTn ($n \geqslant 1$) controlling scheme is depicted in Fig. 8. In Fig. 8, more than one shrinkage operation **S** appear since multiple patterns at different scale (i.e., CT0, CT1, and CT2) are to be controlled. Because the shrinkage operations should be applied over scales, the method described in Fig. 8 will be called the hierarchical wavelet shrinkage method. Meanwhile, controlling CTn patterns for multiple n values necessitates the use of a logical operator "AND" but this logical operator is not suitable for a gradient-based optimizer. Therefore, we must develop a scheme to make the "AND" operator differentiable (at least approximately).

In this section, the following schemes are developed to implement the hierarchical wavelet-shrinkage method:

- Pattern detection algorithm using wavelet coefficients
- Hierarchical shrinkage method
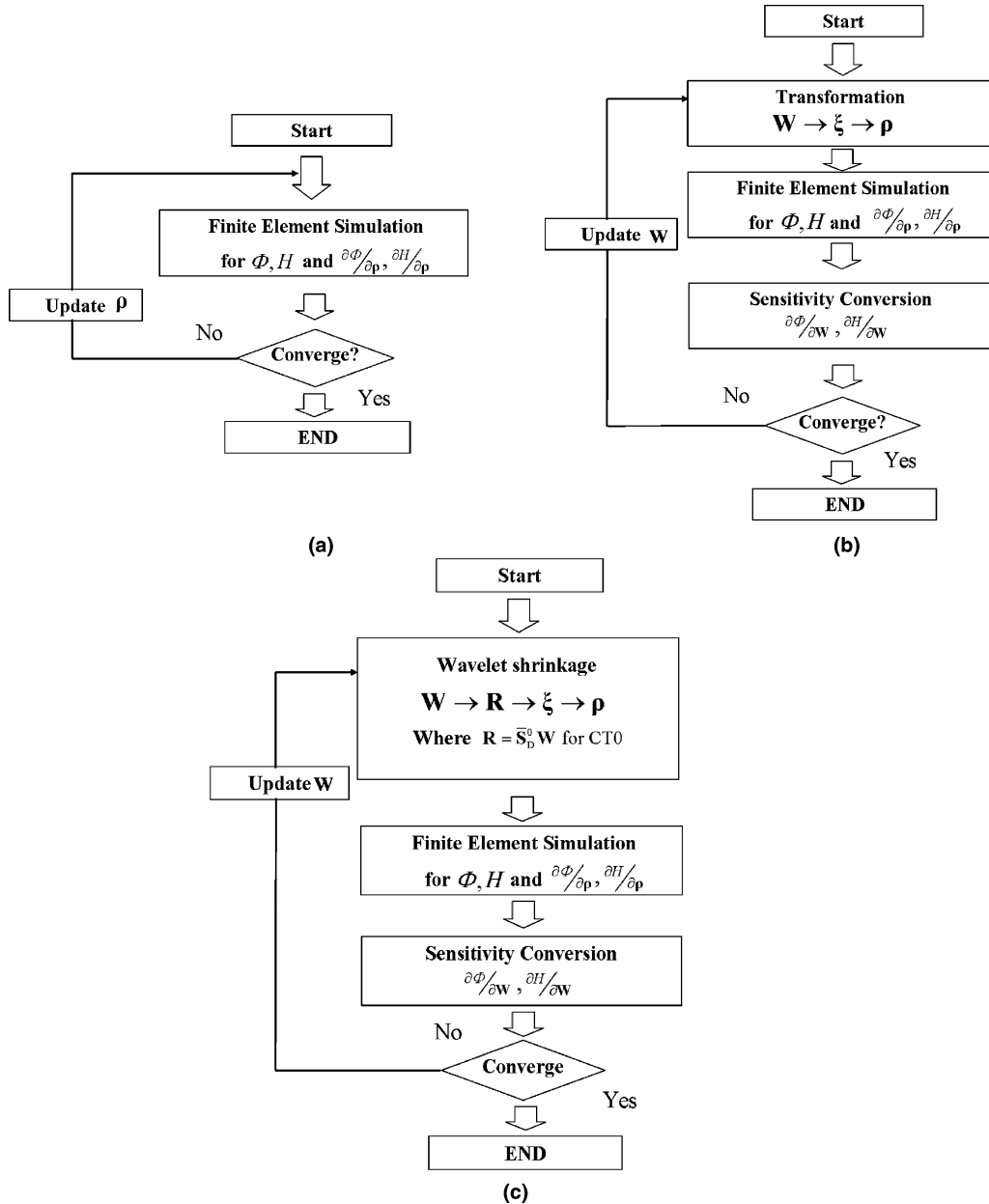- Differentiable version of the logical operator, "AND"

Fig. 7. Flow charts for various topology optimization schemes. (a) Standard topology optimization, (b) multiscale topology optimization, and (c) the wavelet-shrinkage multiscale topology optimization for hinge-free designs. (Note that the wavelet space, $\mathbf{W}$, is shrunk by the shrinkage operator $\overline{\mathbf{S}}_D^0$ for the reduced space $\mathbf{R}$. The shrinkage operators, including $\overline{\mathbf{S}}_D^0$, will be explained in the next section.)

3.1. Patterns thickness

When a square patch is examined for thickness control, it is convenient to introduce the notion of patch lengths. The minimum diagonal length of the solid part of a square will be defined as L_{min}^d whereas
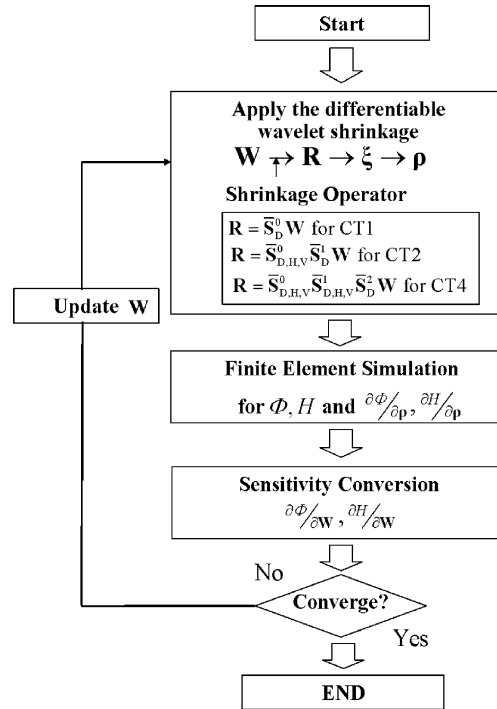
Fig. 8. An overview of the hierarchical wavelet shrinkage method developed to keep the minimum structural connection at CT4. (The meaning of the shrinkage operators, $\overline{\mathbf{S}}^0_{\mathrm{D,H,V}}$, $\overline{\mathbf{S}}^1_{\mathrm{D}}$, and etc., is given in Section 3.2.)

the minimum of the horizontal or vertical length of the solid part will be defined as $L^{\mathrm{h,v}}_{\mathrm{min}}$. As an example, consider a 2×2 patch shown in Fig. 9.

In this case,

$$L^{\mathrm{d}}_{\mathrm{min}} = \sqrt{2} \tag{11}$$

$$L^{\mathrm{h,v}}_{\mathrm{min}} = 1 \tag{12}$$

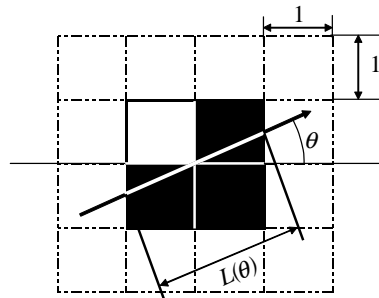

Fig. 9. An example of a 2×2 square patch.

If the minimum connection is set as CT1, then L_{min}^d and $L_{min}^{h,v}$ of all possible 2×2 patches within the design domain must satisfy

$$L_{min}^d \geqslant \sqrt{2} \quad \text{and} \quad L_{min}^{h,v} \geqslant 1 \tag{13}$$

If the minimum connection is set as CT2, the following conditions must be satisfied simultaneously:

$$\text{for all } 4 \times 4 \text{ patches:} \quad L_{min}^d \geqslant 2\sqrt{2} \text{ and } L_{min}^{h,v} \geqslant 2 \tag{14}$$

and

$$\text{for all } 2 \times 2 \text{ patches:} \quad L_{min}^d \geqslant \sqrt{2} \text{ and } L_{min}^{h,v} \geqslant 1 \tag{15}$$

For future use, the condition for the minimum connection to be CTn with $n = 4$ is also stated:

$$\text{for all } 8 \times 8 \text{ patches:} \quad L_{min}^d \geqslant n\sqrt{2} \text{ and } L_{min}^{h,v} \geqslant n \tag{16}$$

$$\text{for all } 4 \times 4 \text{ patches:} \quad L_{min}^d \geqslant \frac{n\sqrt{2}}{2} \text{ and } L_{min}^{h,v} \geqslant \frac{n}{2} \tag{17}$$

and

$$\text{for all } 2 \times 2 \text{ patches:} \quad L_{min}^d \geqslant \frac{n\sqrt{2}}{4} \text{ and } L_{min}^{h,v} \geqslant \frac{n}{4} \tag{18}$$

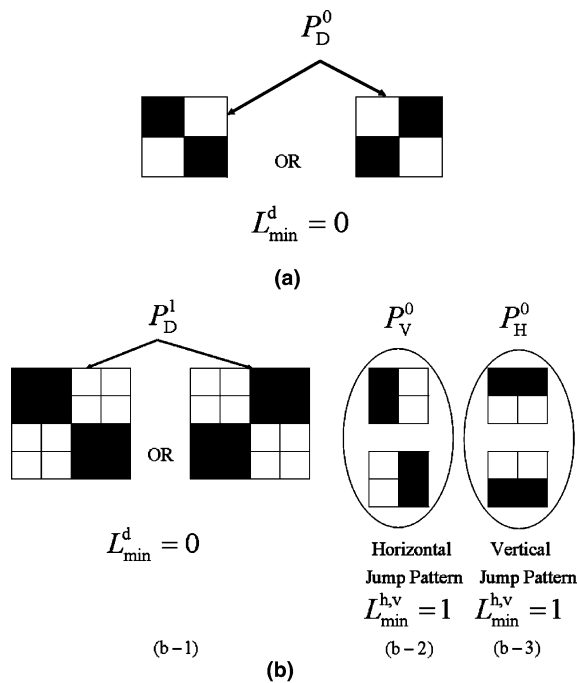For CTn ($n \geqslant 5$), conditions similar to Eqs. (16)–(18) can be used.

Fig. 10. Patterns to be checked and controlled.

To bring the notion of the minimum structural connection to our attention, let us consider patterns in Fig. 10. If the minimum structural connection is set as CT1, the pattern shown in Fig. 10(a) will be checked and suppressed. When the minimum structural connection is set as CT2, the patterns in Fig. 10(b) must be controlled. In addition, the pattern in Fig. 10(a) should be also controlled.

Imposing the minimum structural connection at CT2 and CTn ($n \geqslant 3$) is not so easy because the finite element discretization resolution is not the same as the resolution of the controlled pattern. Let us consider the case of Fig. 10(b-1) where the resolution of the hinge pattern is lower than the resolution of the finite element discretization. One may simply suppress the hinge pattern of Fig. 10(b-1) in order to impose the minimum structural connection at CT2. Due to inevitable numerical errors occurring during the shrinkage and optimization process, however, patterns belonging to CT1 such as Fig. 10(b-2) and (b-3) cannot be completely suppressed. The reason for this phenomenon will be given in the subsequent discussion along with a method to control the minimum thickness at a desired scale. For future reference, the pattern in Fig. 10(b-2) and (b-3) will be referred to as the horizontal jump pattern and the vertical jump pattern, respectively.

3.2. Pattern detection algorithm in the wavelet space

In order to control patterns in the wavelet space, a pattern detection algorithm should be expressed in terms of wavelet variables. Let us begin with considering square patches defined in the space of ξ, as illustrated in Fig. 11.

The superscript j in ξ_i^j in Fig. 11 denotes the resolution level and the variable d is introduced to represent the difference between two adjacent variables ξ_i^j:

Local horizontal differences:

$$\begin{aligned} d_1^j &= \xi_1^j - \xi_2^j = w_4^j - w_2^j \\ d_3^j &= \xi_4^j - \xi_3^j = w_2^j + w_4^j \end{aligned} \tag{19}$$

Local vertical differences:

$$\begin{aligned} d_2^j &= \xi_2^j - \xi_4^j = -w_3^j - w_4^j \\ d_4^j &= \xi_3^j - \xi_1^j = w_3^j - w_4^j \end{aligned} \tag{20}$$

Note that all d_i^j variables can be written compactly in terms of the wavelet variables w_i^j at any resolution level. Based on the variables d_i^j, the following criteria are proposed to identify patterns of Fig. 10(a), (b-2), and (b-3):

$$\text{Criterion I:} \quad (d_1^i)^2 + (d_2^i)^2 + (d_3^i)^2 + (d_4^i)^2 < \varepsilon \tag{21}$$

$$\text{Criterion II:} \quad d_1^i \times d_2^i \geqslant 0 \ \text{ or } \ d_2^i \times d_3^i \geqslant 0 \ \text{ or } \ d_3^i \times d_4^i \geqslant 0 \ \text{ or } \ d_4^i \times d_1^i \geqslant 0 \tag{22}$$

$$\text{Criterion III:} \quad (d_2^i)^2 + (d_4^i)^2 > D_{\text{upper}} \ \text{ and } \ (d_1^i)^2 + (d_3^i)^2 < D_{\text{lower}} \tag{23}$$

$$\text{Criterion IV:} \quad (d_2^i)^2 + (d_4^i)^2 < D_{\text{lower}} \ \text{ and } \ (d_1^i)^2 + (d_3^i)^2 > D_{\text{upper}} \tag{24}$$

(Typical values of ε, D_{lower}, D_{upper}: $\varepsilon = 144$, $D_{\text{lower}} = 25$, $D_{\text{upper}} = 800$).

Criterion I and II have been used in Yoon et al. (2004) and Criterion III and IV are newly introduced here. Criterion I checks any appreciable pattern variation, and Criterion II checks the monotonousness of a square patch. Therefore, if a square patch is a hinge pattern, neither Criterion I nor II is satisfied. Similarly,

(a) Patch at Level 0
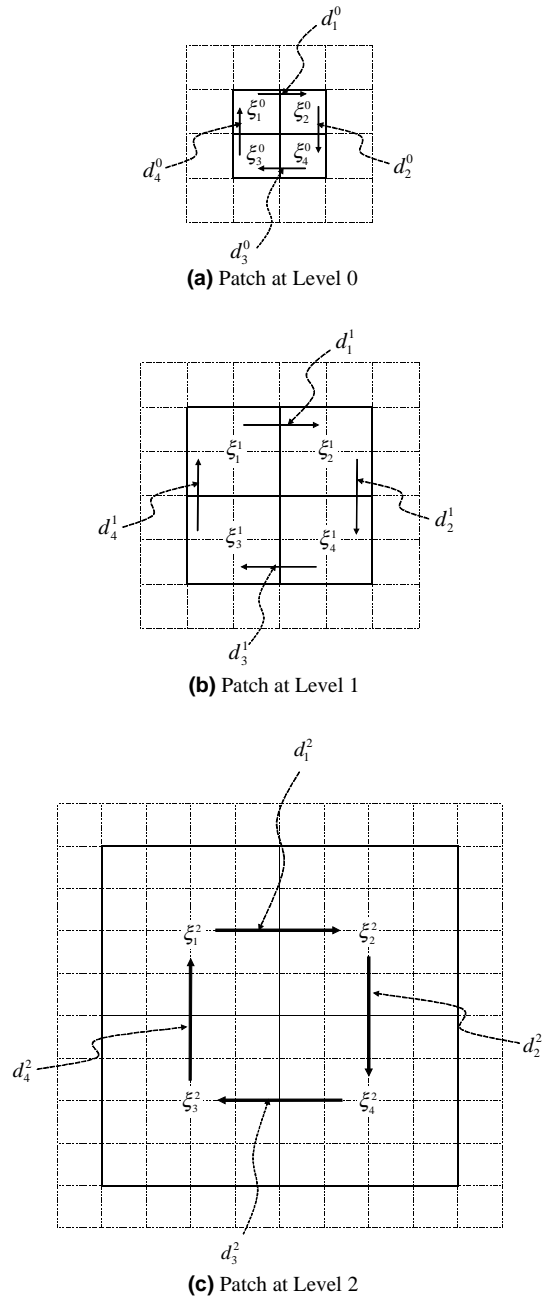
(b) Patch at Level 1

(c) Patch at Level 2

Fig. 11. Square patches at various resolution levels. (The lowest resolution level is level 0.)

since $(d_1^i)^2 + (d_3^i)^2$ and $(d_2^i)^2 + (d_4^i)^2$ quantify the horizontal difference and the vertical difference, respectively, Criterion III and IV can be used to detect the vertical and horizontal jump patterns, respectively. The proposed pattern detection algorithm is summarized in Box 1.

Box 1. Basic pattern detection algorithm applied to a square patch P^j discretized by $2^{j+1} \times 2^{j+1}$ elements.

If $\{f_{\mathrm{I}} < 0$ or $(f_{\mathrm{II}}^1 > 0$ or $f_{\mathrm{II}}^2 > 0$ or $f_{\mathrm{II}}^3 > 0$ or $f_{\mathrm{II}}^4 > 0)\}$
    P^j is not declared as P_{D}^j. (P_{D}^j: Hinge Pattern)
If $\{f_{\mathrm{III}}^1 \leqslant 0$ and $f_{\mathrm{III}}^2 \geqslant 0)$
    P^j is declared as P_{V}^j. (P_{V}^j : Vertical Jump Pattern)
If $\{f_{\mathrm{IV}}^1 \leqslant 0$ and $f_{\mathrm{IV}}^1 \geqslant 0)$
    P^j is declared as P_{H}^j. (P_{H}^j: Horizontal Jump Pattern)
where

$$f_{\mathrm{I}} = (d_1^i)^2 + (d_2^i)^2 + (d_3^i)^2 + (d_4^i)^2 - \varepsilon$$

$$f_{\mathrm{II}}^1 = d_1^i \times d_2^i, \ \ f_{\mathrm{II}}^2 = d_2^i \times d_3^i, \ \ f_{\mathrm{II}}^3 = d_3^i \times d_4^i, \ \ f_{\mathrm{II}}^4 = d_4^i \times d_1^i$$

$$f_{\mathrm{III}}^1 = (d_1^i)^2 + (d_3^i)^2 - D_{\mathrm{lower}}, \ \ f_{\mathrm{III}}^2 = (d_2^i)^2 + (d_4^i)^2 - D_{\mathrm{upper}}$$

$$f_{\mathrm{IV}}^3 = (d_2^i)^2 + (d_4^i)^2 - D_{\mathrm{lower}}, \ \ f_{\mathrm{IV}}^4 = (d_1^i)^2 + (d_3^i)^2 - D_{\mathrm{upper}}$$

with

$$d_1^i = w_4^i - w_2^i, \ \ d_2^i = -w_3^i - w_4^i, \ \ d_3^i = w_2^i + w_4^i, \ \ d_4^i = w_3^i - w_4^i$$

In order to convey the underlying ideal of the algorithm in Box 1, let us consider the patches in Fig. 12.

Case 1: Hinge pattern detection by the algorithm in Box 1.
When the criterion of Eq. (21) is checked, the patch in Fig. 12(a) can be identified as a hinge pattern P_{D}^0.

$$\rho : \begin{bmatrix} 0.99753 & 0.00247 \\ 0.00247 & 0.99753 \end{bmatrix} \rightarrow \xi : \begin{bmatrix} 20 & -20 \\ -20 & 20 \end{bmatrix}$$

$$d_1^0 = 40, \quad d_2^0 = -40, \quad d_3^0 = 40, \quad \text{and} \quad d_4^0 = -40 \tag{25}$$

Since $(d_1^0)^2 + (d_2^0)^2 + (d_3^0)^2 + (d_4^0)^2 = 6400 > \varepsilon = 144$, P_1 is declared as P_{D}^0.
Case 2: Vertical jump pattern.
When the Criterion III of Eq. (23) is satisfied, a patch in Fig. 12(b) and Eq. (26) can be categorized as a vertical jump pattern P_{V}^0.
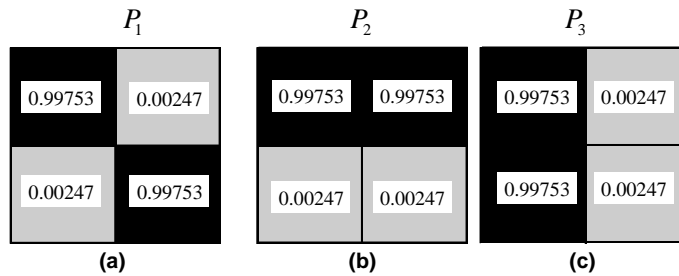

Fig. 12. The simplest numerical examples. (a) Hinge pattern, (b) vertical jump pattern, and (c) horizontal jump pattern.

$$\rho : \begin{bmatrix} 0.99753 & 0.99753 \\ 0.00247 & 0.00247 \end{bmatrix} \rightarrow \xi : \begin{bmatrix} 20 & 20 \\ -20 & -20 \end{bmatrix}$$

$$d_1^0 = 0, \quad d_2^0 = 40, \quad d_3^0 = 0, \quad \text{and} \quad d_4^0 = -40 \tag{26}$$

Since $(d_2^0)^2 + (d_4^0)^2 = 3200 > D_{\text{upper}}$ and $(d_1^0)^2 + (d_3^0)^2 = 0 < D_{\text{lower}}$, P_2 is declared as P_V^0.

Case 3: Horizontal jump pattern.

When the Criterion III of Eq. (24) is satisfied, the Patch in Fig. 12(c) and Eq. (27) can be identified as a horizontal jump pattern P_H^0.

$$\rho : \begin{bmatrix} 0.99753 & 0.00247 \\ 0.99753 & 0.00247 \end{bmatrix} \rightarrow \xi : \begin{bmatrix} 20 & -20 \\ 20 & -20 \end{bmatrix}$$

$$d_1^0 = 40, \quad d_2^0 = 0, \quad d_3^0 = -40, \quad \text{and} \quad d_4^0 = 0 \tag{27}$$

Since $(d_1^0)^2 + (d_3^0)^2 = 3200 > D_{\text{upper}}$ and $(d_2^0)^2 + (d_4^0)^2 = 0 < D_{\text{lower}}$, P_3 is declared as P_H^0.

3.3. Hierarchical shrinkage method

To impose the minimum structural connection at CTn ($n \geqslant 2$), the shrinkage method based on the pattern detection algorithm (Box 1) should be applied hierarchically. If the shrinkage operation is used to suppress CT0 patterns, the minimum connection will become CT1. If only CT0 patterns are to be suppressed, only P_D^0 patterns (in Fig. 13) need to checked, and thus the shrinkage operator S_D^0 representing Eqs. (9) and (10) is used to restrict W as

$$\text{CT1}: \quad R = S_D^0 W \tag{28}$$

In S_D^0, the superscript 0 denotes the highest resolution level and the subscript D, the diagonal pattern, i.e., the well-known hinge pattern. Therefore, all 2×2 patches at the highest resolution are checked and the 2×2 hinge patterns are suppressed by the application of S_D^0 to W. Therefore, the original design space is restricted to a design space free from CT0.

To clarify the role of the shrinkage operation, we will consider all possible patterns that can appear on 2×2 patches as illustrated in Fig. 13. There are $2^4 = 16$ different patterns, but the application of the wavelet shrinkage operation by Eq. (28) suppresses the formation of P_D^0 (the finest diagonal patterns). Thus, 14 patterns, out of 16 patterns, survive after the application of S_D^0. (Though black pixels in Fig. 13 represent the presence of solid material in that location, the actual state during optimization may be somewhere between a solid state and a void state.)
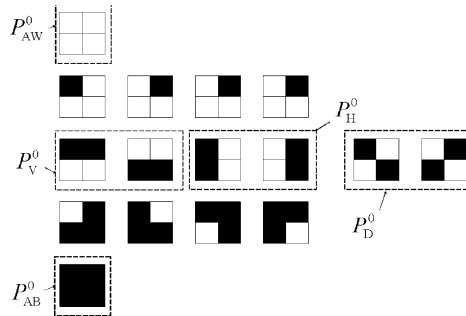

Fig. 13. All possible 16 patterns that can be formed on 2×2 patches.

To control the minimum structural connection at CT2 or CT4, the following hierarchical shrinkage operations are proposed:

CT2: $\mathbf{R} = \mathbf{S}_{\mathrm{D,H,V}}^{0} \mathbf{S}_{\mathrm{D}}^{1} \mathbf{W}$ (29)

CT4: $\mathbf{R} = \mathbf{S}_{\mathrm{D,H,V}}^{0} \mathbf{S}_{\mathrm{D,H,V}}^{1} \mathbf{S}_{\mathrm{D}}^{2} \mathbf{W}$ (30)

To explain the hierarchical shrinkage operations in Eqs. (29) and (30), let us consider a typical patch P^1 in a 4×4 design domain, which is shown in Fig. 14(a).

To make the minimum connection at CT2, P_{D}^{1} patterns (the diagonal patterns of level 1 of Fig. 14(b)) must be suppressed. One may eliminate P_{D}^{1} patterns just as P_{D}^{0} was eliminated, but some care must be taken because the patch resolution is not the same as the resolution of the domain discretization. The difficulty in imposing the minimum connection at CT2 may be demonstrated better by using the illustrations shown in Fig. 15.

In Fig. 15(a), $\bar{\xi}$ denotes a certain value of ξ. All four patterns (Q_1 to Q_4) in the top of Fig. 15(a) should be eliminated from the design space to impose the minimum connection at CT2. However, only the first pattern Q_1 can be completely removed if P_{D}^{1} is suppressed. In order to show this phenomenon, each of the four patterns is decomposed into the sum of two patterns in Fig. 15(a). As can be seen in Fig. 15(a), the rest three patterns (Q_2, Q_3, Q_4) still have additional patterns to be removed even after the elimination of the low-resolution P_{D}^{1} pattern. Again, this phenomenon results from the difference in the patch resolution and the discretization resolution. Therefore, if a P^1 patch is declared as P_{D}^{1}, then its child patches, as defined in Fig. 15(b), should not contain any of P_{D}^{0} (the hinge pattern), P_{H}^{0} (the horizontal jump pattern), or P_{V}^{0} (the vertical jump pattern). Therefore, when P^1 is declared as P_{D}^{1}, the shrinkage process must eliminate P_{D}^{1}. In addition, the process must eliminate the child patterns P_{D}^{0}, P_{H}^{0} and P_{V}^{0}. This overall shrinkage process is symbolized by $\mathbf{S}_{\mathrm{D}}^{1}$.
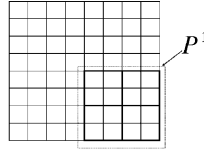
(a) An example of a P^1 patch in a 8×8 design domain
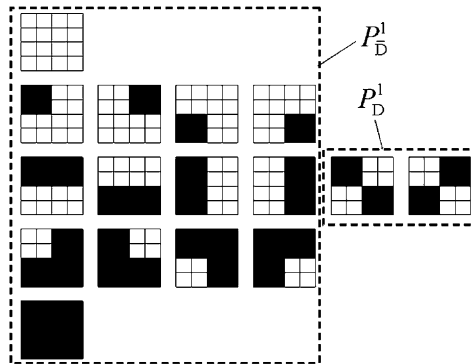
(b) Possible patterns of P^1 in a 4×4 design domain
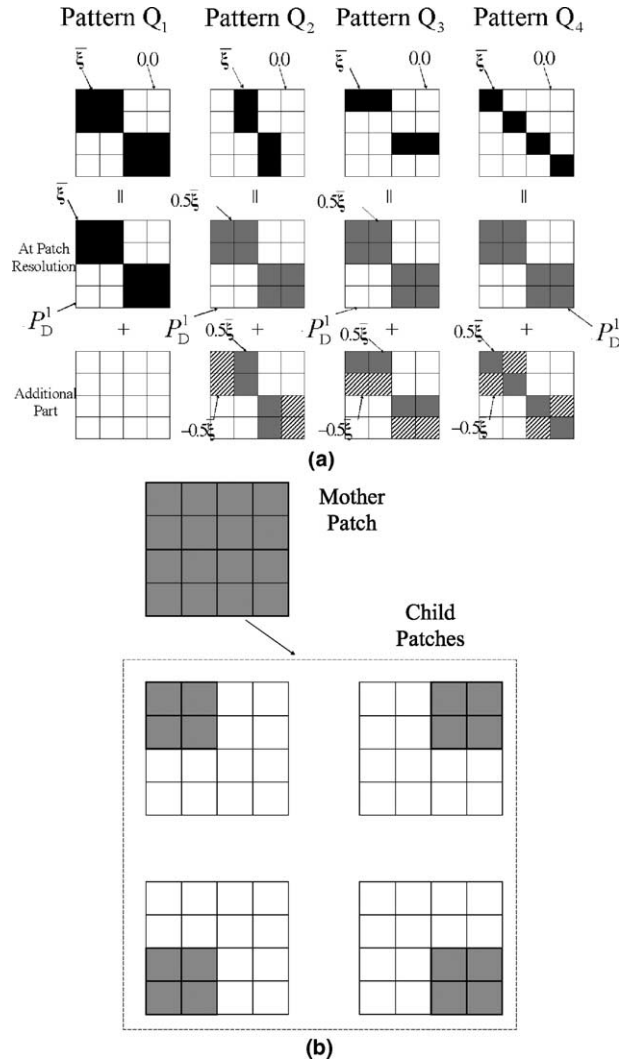
Fig. 14. Illustration of various P^1 patterns.

Fig. 15. Some patterns having the same P_D^1 pattern at the lower patch resolution.

Even after the application of the shrinkage operator $\mathbf{S}_D^1$, sometimes the minimum connection at a patch interfacing two or more P_D^1-free patches does not belong to CT2. These typical situations are illustrated in Fig. 16.

As shown in Fig. 16, not every P^1 patch (4×4 patch) is P_D^1, but some connections may have scales shorter than CT2. Since P_D^0, P_H^0, and P_V^0 illustrated in Fig. 16 are not the child patches of P^1, the suppression of P_D^0, P_H^0, and P_V^0 must be carried out in addition to the suppression of P_D^1. This additional operation followed by the operation $\mathbf{S}_D^1$ is denoted by $\mathbf{S}_{D,H,V}^0$ in Eq. (29).

If the minimum structural connection is set as CT4, then the shrinkage operation stated as Eq. (30) will be used. Because the shrinkage operation is achieved over multiple scales, from long-scale patterns to short-scale patterns, the shrinkage operation is called hierarchical. The hierarchical shrinkage operation process is summarized as Box 2.
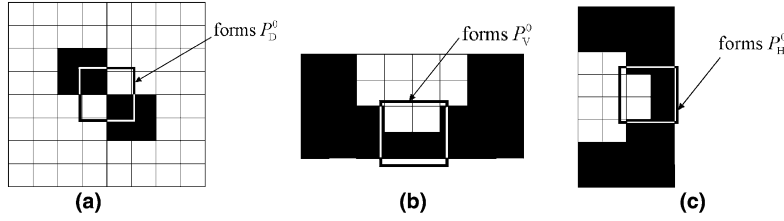
Fig. 16. Some situations where P_D^0, P_H^0, or P_V^0 appears even if P^1 patches are P_D^1-free.

Box 2. Hierarchical shrinkage algorithm.

```
CL = m of CTn (where n = 2^m)
While (CL ⩾ 0)
{
   if(CL = m)
   shrink_patterns='D'
   else
   shrink_patterns='D, H, V'
   Examine the entire design domain
   {
      Select "shrink_patterns" using the algorithm in Box 1
      Also select the child group index
      Shrink the corresponding wavelet variables by Eqs. (28)–(30)
      Also shrink the child wavelet variables if the mother patch is shrunk
   }
   Decrease CL by one
}
```

3.4. Differentiable hierarchical shrinkage operator

Because the shrinkage operations involve logical operators such as "AND and "OR" (see Box 1), the operations cannot be directly incorporated into gradient-based optimizers. To overcome this difficulty, re-laxed differentiable versions of logical operators should be developed by extending the idea used in Yoon et al. (2004). This section is devoted to the development of approximate differentiable versions of all logical statements.

Suppose that the following expressions are given with logical variables, A through E:

$$C = A \text{ OR } B \tag{31}$$

$$D = A \text{ AND } B \tag{32}$$

$$E = \text{NOT } A \tag{33}$$

where

$$A = \text{EXP} = f_A(x_i) > 0 \tag{34}$$

By definition, a logical variable A becomes 1 if EXP (EXP stands for an expression) is true, or zero otherwise. In all cases, we assume that EXP is stated by greater-than inequalities.

Let a, b, c, d, and e be relaxed differentiable logical variables corresponding to A, B, C, D, and E. We design "a" in such a way that it takes a value sufficiently close to 1 when f_A is true, and a value sufficiently close to zero when f_A is not true. Furthermore, the logical variable "a" should be differentiable with respect to any variable appearing in f_A.

The key function to devise the relaxed differentiable versions of logical operations is the sigmoid function, $LSF(x)$ having the following form:

$$y = LSF(z) = \frac{1}{1 + e^{-sz}} = \begin{cases} \approx 1 & \text{if } z > 0 \\ 0.5 & \text{if } z = 0 \\ \approx 0 & \text{if } z < 0 \end{cases} \quad (\text{say}, s = 300) \tag{35}$$

Unless the value of z is very close to 0, $LSF(z)$ gives values very close to either 0 or 1.

By means of LSF, one may express a differentiable version of Eq. (34):

$$a = LSF(f_A(x_i)) \tag{36}$$

Note that any expression involving "IF" can be made differentiable by Eq. (36). By utilizing LSF again, one can write the differentiable version of logical expressions involving "OR", "AND" and "NOT" as

$$\text{The differentiable OR operator:} \quad c = LSF(a + b - \delta) \tag{37}$$

$$\text{The differentiable AND operator:} \quad d = LSF(a \cdot b - \delta) \tag{38}$$

$$\text{The differentiable NOT operator:} \quad e = 1 - LSF(a) \tag{39}$$

where δ is a shifting parameter. The value of $\delta = 0.05$ will be used unless stated otherwise. The behavior of "d" corresponding to D involving an "AND" operator is plotted in Fig. 17. The actual numerical values for various combinations of (a,b) are given below.

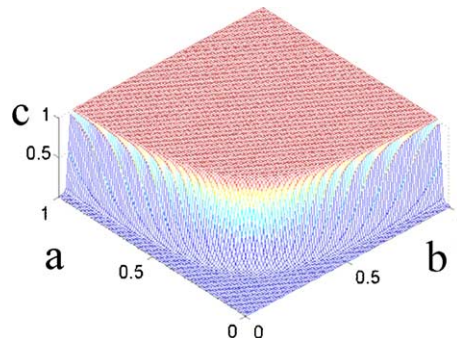| c	a	b
1.00000	1.000	1.000
3.05802×10^{-7}	1.000	0.000
3.05802×10^{-7}	1.000	0.000
3.05802×10^{-7}	0.000	0.000

Fig. 17. The behavior of the differentiable "c" of Eq. (31) involving an "AND" operator where "a" and "b" are differentiable logical variables.

To show the differentiability of the proposed logical variables, let us assume that f_A and f_B are functions of two real variables x_1 and x_2. In this case, the differentiable logical variable "d," for instance, also becomes a function of x_1 and x_2 as

$$d(x_1, x_2) = \text{LSF}(\text{LSF}(f_A(x_1, x_2)) \times \text{LSF}(f_B(x_1, x_2)) - \delta) \tag{40}$$

It is obvious from Eq. (40) that the differentiation of "d" with respect to real variables x_i can be obtained in closed form. When the differentiable logical operations of Eqs. (35)–(39) are employed, the wavelet shrinkage algorithm to impose the minimum connection at CT1 can be expressed as the algorithm in Box 3. To impose the minimum connection at CT2, the hierarchical differentiable shrinkage algorithm proposed in Box 4 can be used.

Box 3. Differentiable shrinkage algorithm to impose the minimum connection at CT1.

$$
\begin{aligned}
&r_1^0 = w_1^0 \\
&r_i^0 = \text{sh}_\text{D}(w_2^0, w_3^0, w_4^0)w_i^0 \ (i = 2, 3, 4) \\
&\text{where} \\
&\text{sh}_\text{D}(w_2^0, w_3^0, w_4^0) = 1 - \text{LSF}(-c_1^0 - c_2^0 + \delta) \\
&\quad c_1^0 = \text{LSF}(-f_\text{I}) \\
&\quad c_2^0 = \text{LSF}(\sum_{j=1}^{4} LSF(f_\text{II}^j) - \delta) \\
&(f_\text{I}, f_\text{II}^j: \text{defined in Box 1.})
\end{aligned}
$$

If needed, the hierarchical shrinkage algorithm in Box 4 can be easily extended to impose the minimum connection at any CTn. However, the scaling properties of the wavelet limits restrict n to be some power of 2 (i.e., $n=1, 2, 4, 8, \ldots$).

Box 4. Hierarchical shrinkage algorithm to impose the minimum connection at CT2.

$$
\begin{aligned}
&r_1^1 = w_1^1 \\
&r_i^1 = \text{sh}_\text{D}(w_2^1, w_3^1, w_4^1)w_i^1 \ (i = 2, 3, 4) \\
&\text{where} \\
&\quad \text{sh}_\text{D}(w_2^1, w_3^1, w_4^1) = 1 - \text{LSF}(-c_1^1 - c_2^1 + \delta) \\
&\quad c_1^1 = \text{LSF}(-f_\text{I}) \\
&\quad c_2^1 = \text{LSF}(\sum_{j=1}^{4} \text{LSF}(f_\text{II}^j) - \delta) \\
&r_i^0 = \text{sh}_\text{H,V,D}(w_2^0, w_3^0, w_4^0)w_i^0 \ (i = 2, 3, 4) \\
&\text{where} \\
&\quad \text{sh}_\text{H,V,D}(w_2^0, w_3^0, w_4^0) = 1 - \text{LSF}(is\_d + is\_hv - \delta) \\
&\quad is\_d = \text{LSF}(-c_1^0 - c_2^0 + \delta) \\
&\quad\quad c_1^0 = \text{LSF}(-f_\text{I}) \\
&\quad\quad c_2^0 = \text{LSF}(\sum_{j=1}^{4} \text{LSF}(f_\text{II}^j) - \delta) \\
&\quad is\_hv = \text{LSF}(v + h - \delta) \\
&\quad\quad h = \text{LSF}(\text{LSF}(-f_\text{III}^1) \times \text{LSF}(f_\text{III}^2) - \delta) \\
&\quad\quad v = \text{LSF}(\text{LSF}(-f_\text{IV}^1) \times \text{LSF}(f_\text{IV}^2) - \delta) \\
&(f_\text{I}, f_\text{II}^j, f_\text{III}^1, f_\text{III}^2, f_\text{IV}^1, f_\text{IV}^2: \text{defined in Box 1.})
\end{aligned}
$$

3.5. Remark on the translation-invariant issue

Although the pattern recognition with wavelet variables is very effective, the direct application of the shrinkage method described in the previous section may fail to detect all patterns to be eliminated. This is because the wavelet basis at a given scale is constructed only by the 2^n translations of one wavelet in the horizontal, vertical and diagonal directions. This problem arises from the translation-variant property of the wavelet basis. To overcome this, Yoon et al. (2004) have developed a method to detect all unwanted patterns, which is called the non-redundant translation-invariant wavelet shrinkage method. Since the translation-invariant method and the algorithm implementation by Yoon et al. (2004) are equally applicable to the hierarchical wavelet shrinkage developed here, the detailed account of the method will not be repeated. To emphasize the translation-invariant property, we will denote the non-redundant translation-invariant version of $\mathbf{S}$ by $\overline{\mathbf{S}}$. Therefore, Eqs. (28)–(30) should be replaced as

$$\text{CT1}: \quad \mathbf{R} = \overline{\mathbf{S}}_{\mathrm{D}}^{0}\mathbf{W} \tag{41}$$

$$\text{CT2}: \quad \mathbf{R} = \overline{\mathbf{S}}_{\mathrm{D,H,V}}^{0}\overline{\mathbf{S}}_{\mathrm{D}}^{1}\mathbf{W} \tag{42}$$

$$\text{CT4}: \quad \mathbf{R} = \overline{\mathbf{S}}_{\mathrm{D,H,V}}^{0}\overline{\mathbf{S}}_{\mathrm{D,H,V}}^{1}\overline{\mathbf{S}}_{\mathrm{D}}^{2}\mathbf{W} \tag{43}$$

4. Case studies

Two topology optimization problems were studied in this section: the design of thermal actuators and the design of electro-thermal-compliant actuators where the minimum thickness control at various scale levels was taken into account. The method of moving asymptotes by Svanberg (1987) was used as a gradient-based optimizer for all numerical problems.

4.1. Thermal actuator design with minimum thickness control

The objective of this design problem is to find an optimal layout that maximizes the displacement at A under a uniform temperature rise by ΔT on three shaded boundaries:

$$\begin{aligned} \text{maximize} \quad & \Phi = U_{\mathrm{A}} \\ \text{subject to} \quad & H = \sum_{e=1}^{NE} \rho_e v_e - M_0 \leqslant 0 \end{aligned} \tag{44}$$

For future use, a simple conceptual actuator configuration is also given in Fig. 18(b). The optimized thermal actuators that are obtained by the developed hierarchical wavelet shrinkage topology optimization are shown in Fig. 19. Due to the symmetry, only half of the design domain is discretized by 8192 four-node finite elements. The layouts in Fig. 19(b)–(d) were obtained by employing the shrinkage operations in Eqs. (41)–(43), each of which imposes the minimum connection thickness at CT1, CT2, or CT4.

The results in Fig. 19 indicate that the developed hierarchical wavelet shrinkage successfully gives the layouts having the desired minimum connection sizes. Interestingly, an optimized result almost similar to the one shown in Fig. 18(b) was obtained when the minimum connection was imposed at CT4. The optimized designs in Fig. 19 suggest that the developed method is capable of controlling the minimum thickness at a desired scale level. It is also shown that as n of CTn becomes larger, the value of U_{A} reduces. This behavior agrees well with our physical intuition. The appearance of some isolated parts seen in Fig.
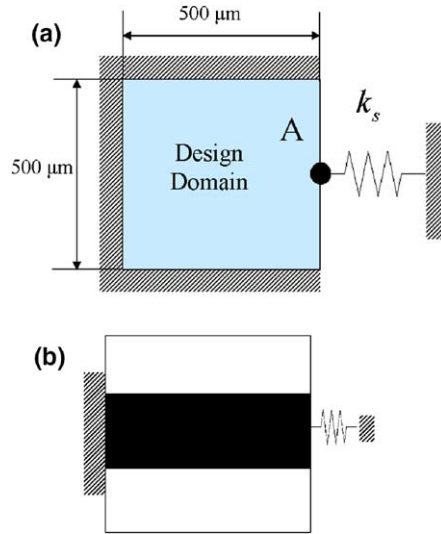
Fig. 18. (a) The problem definition for the design problem of thermal actuators ($k_s = 80$ N/mm, mass constraint = 25%, Young's modulus = 200 GPa, Poisson's ratio = 0.31, depth = 15 μm, $\Delta T = 500$ K, thermal expansion coefficient = 15×10^{-6} K^{-1}) and (b) a conceptual thermal actuator.
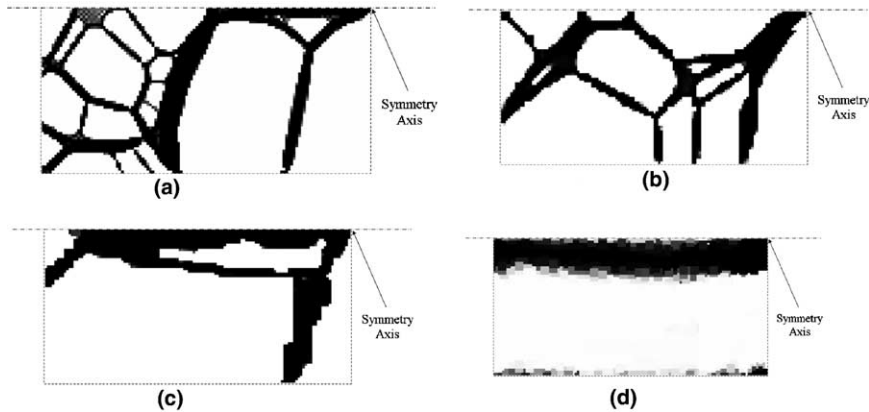

Fig. 19. The optimized layouts of thermal actuators (no postprocessing used). (a) No minimum connection size control ($U_A = 3.25$ μm), (b) the minimum connection imposed at CT1 ($U_A = 2.92$ μm), (c) CT2 ($U_A = 2.19$ μm), (d) CT4 ($U_A = 1.89$ μm).

19(c) and (d) is due to the periodic condition used for the wavelet transformation. Similar problems were also observed when the wavelet based method was used to control the topological complexity of an optimized result by the topology optimization method (Seo and Kim, 2005).

4.2. Electro-thermal-compliant actuator design with minimum thickness control

As the second design problem, the topology design optimization of a microelectro-thermal-compliant actuator was considered. This problem was worked out by Sigmund (2001), but the minimum connection size control at CT2 or CT4 has not been yet solved in the existing investigations. The design problem is
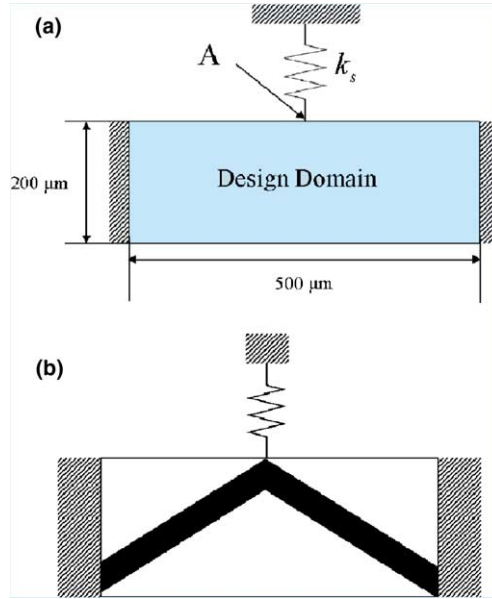
Fig. 20. (a) The problem definition for the design of an electro-thermal-compliant actuator ($k_s = 100$ N/m, Mass constraint = 30%, Young's modulus = 200 GPa, Poisson's ratio = 0.31, depth = 15 μm, the electric conductivity = 6.4×10^6 K(Ω m)$^{-1}$, the thermal conductivity = 90.7 W/(K m), the convection coefficient = 18.7×10^3 W/(m^2 K), thermal expansion coefficient = 15×10^{-6} K^{-1}, applied voltage = 0.3 V) and (b) a conceptual design. (This design was used by Que et al. (2001) and Wang et al. (2003).)

described in Fig. 20(a). The objective of this design problem is to find an optimal layout to maximize the displacement output at A under a given voltage input on the shaded boundaries to the system (see Sigmund (2001), Ananthasuresh et al. (1994), Yin and Ananthasuresh (2002) for the problem formulation):

$$\text{maximize} \quad \Phi = U_A$$

$$\text{subject to} \quad H = \sum_{e=1}^{NE} \rho_e v_e - M_0 \leqslant 0 \tag{45}$$

To solve Eq. (45), coupled electric, thermal, and structural analyses were conducted. In this work, the structure was assumed to behave linearly and displacement-based four-node finite elements were used for the discretization of the design domain.

As in the previous example, we also considered a simple, conceptual electro-thermal-compliant actuator in Fig. 20(b). The actuator design in Fig. 20(b) has been used in the MEMS community (see, e.g., Que et al., 2001; Wang et al., 2003). If the developed hierarchical wavelet shrinkage method works, it should also be able to produce a layout like this one.

The optimized layouts with the control of minimum connection size at various scale levels are plotted in Fig. 21. When the minimum thickness was set as CT1, small-sized cooling ribs were formed in the regions where cooling can improve system performance. This phenomenon was also pointed out by Sigmund (2001). As the minimum connection size became larger, however, the small-sized ribs were forced to disappear, as can be seen in Fig. 21(c) and (d). When the minimum connection was imposed to be at CT4, in particular, the actuator looked like a thick curved beam, which is almost identical to the one shown in Fig. 20(b).

The optimized result in Fig. 21(c) may be considered by a designer as a good design candidate because the system performance and the failure resistance appear to be balanced. To compare the overall system
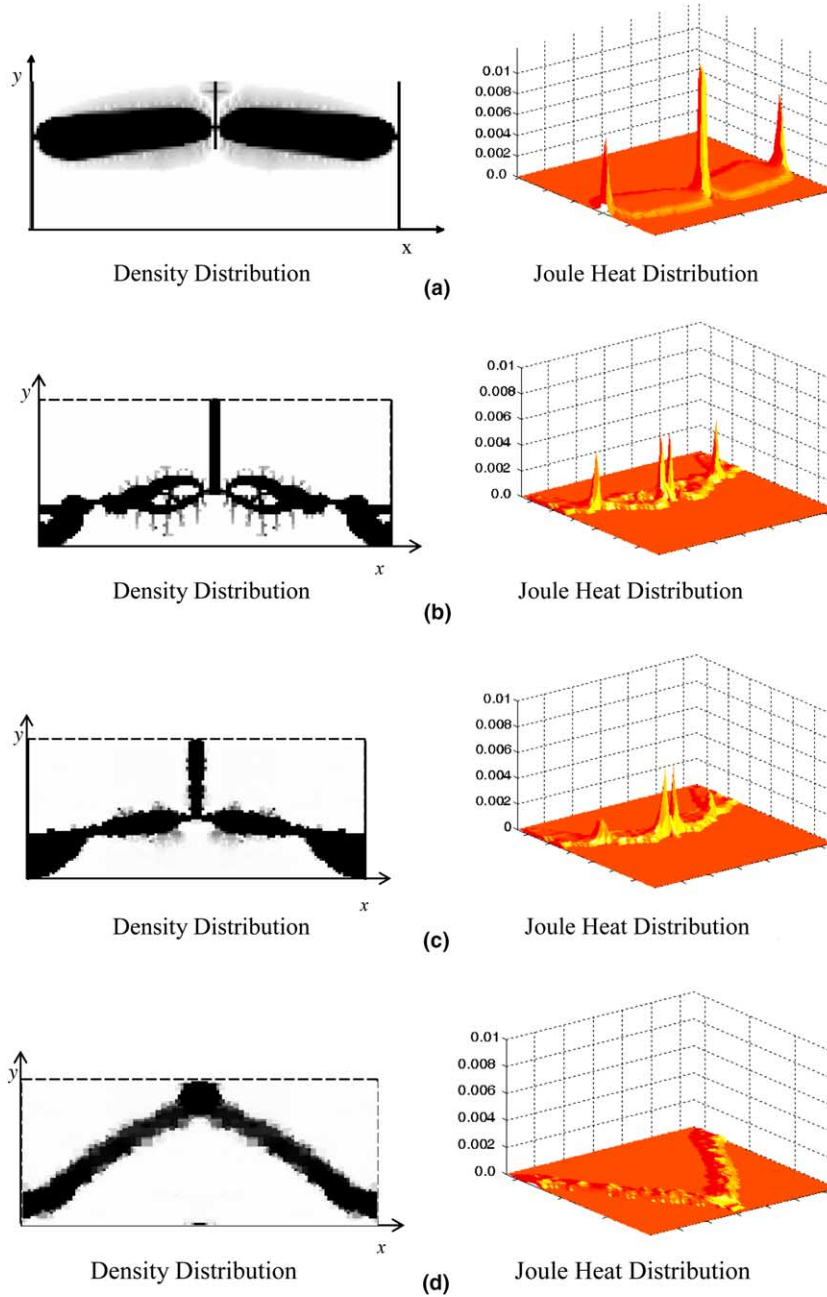
Fig. 21. The optimized result for the electro-thermal-compliant actuator design. (a) No minimum connection size control ($U_A = 13.92\,\mu\text{m}$), the minimum connection imposed at (b) CT1 ($U_A = 6.49\,\mu\text{m}$), (c) CT2 ($U_A = 4.97\,\mu\text{m}$), (d) CT4 ($U_A = 1.23\,\mu\text{m}$) which is similar to the conceptual design by Que et al. (2001) and Wang et al. (2003).

performance of the result in Fig. 21(a) and that of the result in Fig. 21(c), the minimum thickness of the result in Fig. 21(a) is made (manually post-processed) to be the same as that of the result in Fig. 21(c).

The actual design models derived from Fig. 21(a) and (c) are shown by Fig. 22(a) and (b), respectively. For the same input voltage, the output tip displacement, the maximum Von-Mises stress, etc. are compared in Table 1.
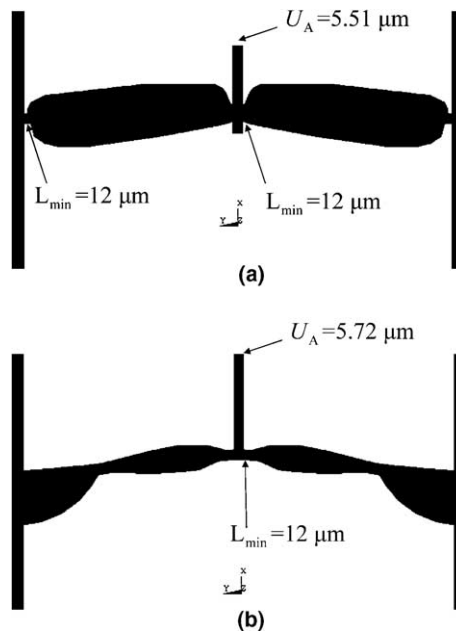

Fig. 22. The design models derived from in Fig. 21. (a) Postprocessed design of the optimized result in Fig. 21(a) to ensure that the minimum thickness is not smaller than 12 μm, (b) from Fig. 21(c).

Table 1
Performance comparison of two designs (for the same voltage input, the same minimum thickness)

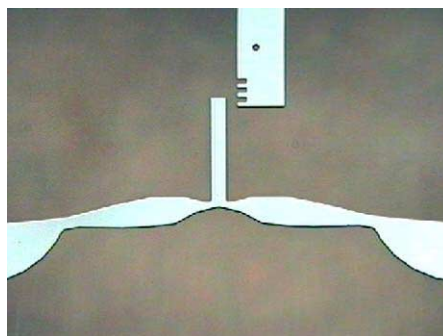| Model	Fig. 23(a)	Fig. 23(b)
U_A	5.51 μm	5.72 μm
Max Von-Mises stress	1.02×10^{10} [N/m^2]	2.18×10^{9} [N/m^2]
Max temperature	673 K	640 K

Fig. 23. A fabricated prototype of the design model in Fig. 22(b).

Table 1 shows that the overall structural performance of the design in Fig. 22(b) is superior to that of the design in Fig. 22(a). These results confirm the importance of the minimum thickness control in improving the overall system performance. Based on the design in Fig. 22(b), a prototype shown in Fig. 23 has been fabricated. An extensive experimental investigation on the system performance of the actuator in Fig. 23 should be conducted, but preliminary experimental tests indicated the usefulness of the proposed minimum thickness controlled topology optimization strategy to reduce failures during fabrication operation stage.

5. Conclusions

In this paper, the minimum thickness control, which is one of the most difficult problems in topology optimization, was studied. A design restriction method called the hierarchical wavelet shrinkage method was developed to control topologically-optimized layouts at a desired minimum thickness scale. To facilitate the minimum thickness control, the topology optimization was carried out in the wavelet design space. Especially when the desired minimum scale is larger than the size of the finite elements used for design domain discretization, the wavelet-shrinkage method should be applied hierarchically. Thus, the implementation strategies of the hierarchical wavelet shrinkage method were developed and applied to a couple of MEMS design problems. Although the suggested method involves somewhat complicated procedures, it produced useful results for the problems considered. The numerical results confirmed the importance of the minimum thickness control during the optimization process. Indeed, the optimized design by the developed controlling method outperformed that of the post-thickened design.

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